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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,029	05/25/2006	Brent A. Anderson	BUR920030082US1	1856

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
08/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,029	ANDERSON ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,12 and 14* is/are rejected.

7)☒ Claim(s) *9,10 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/25/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8, 11-12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6909151 to Hareland et al.

Regarding claim 1, Hareland discloses an integrated circuit semiconductor memory device in fig. 3A-B comprising: a substrate 304; a first dielectric layer 306 covering a first portion of said substrate 304, said first dielectric layer being absent from a second portion of said substrate, fig. 3A; a second dielectric layer 360 or 319 having a property different from said first dielectric layer 306 (oxide vs. nitride), said second dielectric layer 360 at least partly covering said second portion of said substrate 304; a source region 330 formed in a first doped region on said first dielectric layer; a drain region 332 formed in a second doped region on said first dielectric layer; and a gate 324 formed over said second dielectric layer and between said first and second doped regions, wherein said property of said second dielectric layer provides a gate

capacitance of said gate with respect to said substrate that is greater than a theoretical capacitance of a gate formed over said first dielectric layer on said substrate.

With respect to "property of said second dielectric layer provides a gate capacitance of said gate with respect to said substrate that is greater than a theoretical capacitance of a gate formed over said first dielectric layer on said substrate" is a functional limitation. The structure recited in Hareland is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 2-5, Hareland discloses the device wherein said device is RAM, a SRAM, a FET, and a FinFET. A recitation of 'RAM, SRAM, FET and FINFET' does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art-recognized suitability for an intended purpose, MPEP 2144.07. Or such limitations do not carry weight because the limitations are either function or intended use that do not limit the claim to a particular structure, MPEP 2111.04; thus structure of Hareland is capable of performing the same function.

Regarding claims 6, 11, and 14, Hareland discloses wherein said first dielectric layer is a buried oxide layer (SOI), col. 2 line 59, and said second dielectric layer is a thin oxide layer, col. 7 line 24, providing less insulating effect than said buried oxide layer, said gate being capacitively coupled to said substrate.

With respect to "providing less insulating effect than said buried oxide layer, said gate being capacitively coupled to said substrate" is functional limitation. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 7-8, 12, Hareland discloses a fin 308 of said FinFET is formed over said buried oxide layer 306, wherein said device further comprise a gate dielectric layer 322 between said gate 324 and said fin 308, wherein said second dielectric layer has less leakage than said gate dielectric.

With respect to "second dielectric layer has less leakage than said gate dielectric" is functional limitation. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Allowable Subject Matter

3. Claims 9-10 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record neither anticipates nor renders obvious the limitations of claims 9 and 13 including wherein said substrate has an upwardly-facing first surface at an upper level and an upwardly-facing second surface at a lower level, said first dielectric layer being a dielectric layer formed on said first surface, said second dielectric layer being a dielectric layer formed on said second surface, and a fin of said FinFET is formed over said buried layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Primary Examiner, Art Unit 2814